

Nanotechnology: Realizing the Promise of Universal Memory

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ABSTRACT

Nanomaterials are likely to serve as the building blocks for future semiconductor devices. One of the first commercial impacts of nanotechnology on the semiconductor industry could be in the domain of memory. There are three commercially available families of memory: dynamic random access memory (DRAM), static random access memory (SRAM) and nonvolatile memory (Flash). Most consumer and business products use combinations of these three memory families, but there is a growing need for a universal memory that combines the positive attributes of each. In this article, Ben Schlatka examines the key trends and requirements that set the stage for a universal memory. He identifies several possible candidates for universal memory, engages in an in depth analysis of nanotube-based devices, and highlights markets where universal memory could have the greatest impact.

INTRODUCTION

Electronic devices incorporate memory functionality to record, store, and process data, which significantly improves their performance. Memory chips constituted over 46 billion of the 213 billion dollar semiconductor industry in 2004, according to BCC, Inc.¹ The market is composed of primarily three types of memory families: DRAM (dynamic random access memory), SRAM (static RAM) and Flash (nonvolatile memory). DRAM has a small cell size, SRAM is fast, and Flash can store information even when power is turned off. Many of today's consumer and business products use combinations of these three memory families to try to satisfy system level needs. For over thirty years, major corporations and start-ups have been attempting to replace all three of these memory products with a universal memory that combines the positive attributes of each. Today, in addition to the growing technical challenges associated with current memory solutions, the search for a universal memory is intensifying due to the convergence of two major trends.

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¹ See Global Non-Volatile Memory Markets To Cross \$69 Billion By 2012, at [http://www.electronics.ca/PressCenter/articles/94/1/Global-Non-Volatile-Memory-Markets-To-Cross-\\$69-Billion-By-2010](http://www.electronics.ca/PressCenter/articles/94/1/Global-Non-Volatile-Memory-Markets-To-Cross-$69-Billion-By-2010).

Nanotechnology: Realizing the Promise of Universal Memory

The first of these trends relates to Moore's Law. The semiconductor industry doubles the density of transistors in a given area of silicon every 18 months; this steady progression to smaller feature sizes is beginning to place strains on existing memory technologies. In addition, the explosion of mobile devices demanding low power operation and low standby battery drain create a need to commercialize new memory technologies that can deliver these benefits. Together these two trends have catalyzed development efforts in universal memory products that integrate the positive attributes and eliminate the growing technical challenges of existing memory products, while leveraging the billions of dollars that have been invested in CMOS process technology.

This article will examine the key trends and requirements that set the stage for a universal memory. A leading candidate, carbon nanotube based NRAMTM from Nantero, will be reviewed and the initial markets where this product will be most valuable will be examined.

I. TECHNICAL AND MARKET DRIVEN DEVELOPMENT ISSUES

Companies are investigating new forms of memory because existing memory products are facing increasingly difficult technical challenges as the industry moves into successively smaller technology nodes. At the current state of the art, 90nm process node, DRAM and SRAM are beginning to suffer from voltage scaling issues, leakage problems and rising soft error rates. Flash will face challenges due to its process complexity and cell size. Each of these technical issues will be examined in more depth below.

1. Voltage Scaling

Device threshold voltage does not scale well as dimensions shrink. As a result, devices are more difficult to turn OFF, and the stored charge may be lost through leakage. Also, lower voltages mean lower stored charge across the storage capacitor.

2. Leakage Issues

In addition to select device leakage, there is a source diffusion leakage as well. The source diffusion of the select transistor that contacts a terminal of the storage capacitor may leak charge due to silicon substrate crystalline defects. As the number of DRAM bits increase into the billions per chip, this leakage issue becomes more severe. SRAM cells are stable and leakage will not destroy the information as in the DRAM case. However, if leakage current is too high, SRAMs will have an unacceptably high standby current (power) as the number of storage cells increase, which makes their use detrimental to battery dependent devices.

3. Soft Error Rates

Alpha particles from solar radiation striking the silicon substrates in the vicinity of source and drain diffusion regions create hole-electron pairs causing leakage current that can discharge DRAM storage capacitors. SRAM storage cells can also be disturbed by the same mechanism with storage cells flipping to the opposite state. Scaling and increasing the number of bits per device increases the likelihood of this phenomenon.

4. Process Complexity and Cell Size

The insulating silicon dioxide layer in the Flash floating gate architecture serves as a wrapper that stores its charge. This stored charge on the floating gate imparts the nonvolatility feature of Flash. As this insulating layer is continually thinned, charge begins to leak from the device. Conversely, in its existing instantiation, the insulating layer requires excessively large programming voltages to write bits.

As cell size shrinks, it also becomes more likely that high voltages will accidentally program neighboring cells. This high programming voltage makes integration with logic processes extremely difficult.

These technical issues will be exacerbated as the industry continues to shrink feature sizes in devices. The process-driven technical challenges become more significant in the mobile computing paradigm that demands cheap, energy efficient, compact memory technology. Mobile devices that require portability are intensely focused on conserving battery life and thus require very low standby power drain from memory technology. In addition, as more active computing moves into mobile devices, board real estate is becoming more constrained. Employing multiple memory technologies violates all three principles of mobile design by increasing power consumption, adding cost, and reducing design flexibility. The confluence of these two major technical and market trends has catalyzed development efforts to find a memory technology that addresses the major technical challenges of existing memory technology, while combining the value proposition of each - speed, density and nonvolatility.

II. GUIDING PRINCIPLES OF UNIVERSAL MEMORY DEVELOPMENT

The issue of developing a commercially successful memory product depends on more than just the integration of these three features into a single offering. There exists a set of constraints that increases the technical difficulty of this endeavor. For a next generation product to be both technically and commercially viable it must attain the following:

1. Process Qualification

Any new development initiative must be able to leverage the multibillion-dollar investment in manufacturing technology the semiconductor industry makes every several years. This compatibility can be evaluated on several dimensions. New designs must employ materials that can pass the stringent quality and contamination standards in place at leading edge factories today. For example, a facility based on 180nm processing technology requires a contamination level of harmful metals less than 25 parts per billion. Device processing ideally would not require new capital tool purchases, and must not require non-standard tools to be installed in an existing manufacturing line.

2. Process Compatibility

Chip designers often choose to combine memory and logic on one die. Universal memory must be compatible with existing process technologies that support logic based designs. By combining universal memory and logic on one die, designers can increase device performance and reduce power consumption. Integration of memory and logic also result in smaller form factors and higher reliability.

3. Scalability

New devices must demonstrate two types of scalability. They must show a credible path to scaling density within a given technology node and they must all be able to continue to scale to smaller technology nodes, i.e. from a 90nm to a 65nm manufacturing process. These two types of scalability will ensure that the new devices can deliver a reduced cost per bit.

4. Reliability

The semiconductor industry has rigorous reliability standards for its products. New devices must not only work well, but they must also prove they can work well for years under adverse environmental conditions before wholesale commercial adoption will occur in any market segment.

Nanotechnology: Realizing the Promise of Universal Memory

III. UNIVERSAL MEMORY CANDIDATES

There are several emergent memory technologies that attempt to address the aforementioned technical challenges and constraints. They can be segmented into several large categories: magnetic materials based devices, phase change material based devices, ferroelectric material based devices, polymer based devices and carbon nanotube based devices.

Magnetic Materials (MRAM): These memories involve the creation of a tunnel barrier between two magnetic thin film materials. Changing the polarity of the magnetic material causes either a high or low resistance across an insulating barrier, which can be read as a 1 or a 0.

Phase Change/Chalcogenide/Ovonic Materials (CRAM/OUM): Phase change memories employ a material that can exist in two states - an amorphous state which has high resistance and a crystalline state which has a low resistance. Application of heat causes the material to switch from amorphous to crystalline. Bits can be read as a function of high and low resistance when voltage is applied through the material.

Ferroelectric Materials (FRAM): FRAM replaces the standard capacitor in today's DRAM with a ferroelectric crystal, which acts as a capacitor to store data. Non-volatile switching occurs through changes in the polarization of the ferroelectric film. The difference in stored charge between different polarization states distinguishes between an ON and OFF state.

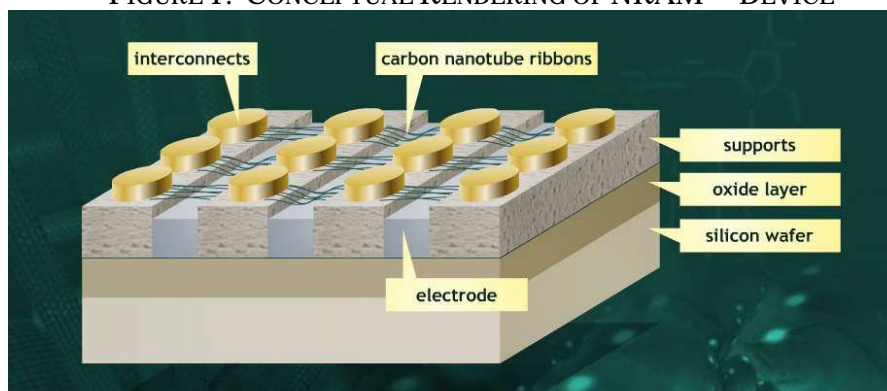
Polymer Materials: Polymer based memories sandwich conductive materials between electrodes. When a field is applied, the resistance of the polymer lowers allowing a charge to pass through the material more easily. This difference in states can be registered as a 1 or a 0. The resistance can be returned to the original state by applying another field.

The following section will describe carbon nanotube based memory, NRAM™, Nantero's answer to the quest for universal memory.

IV. NRAM™ PRINCIPLES OF OPERATION

Nantero's carbon nanotube memory is based on an electromechanical switching principle, balancing three forces: electric, elastic and van der Waals. Ribbons of nanotubes, also referred to as a nanotube fabric, are perpendicularly suspended across trenches etched in silicon wafers and they are anchored to the interconnect. A contact electrode is located in the bottom of the silicon trench.

FIGURE 1: CONCEPTUAL RENDERING OF NRAM™ DEVICE



Source: Nantero, Inc.

When a potential is applied between the fabric and the electrode, the field causes the fabric to bend down and contact an electrode. The fabric will remain stuck to the electrode through molecular surface attractions known as van der Waals forces even when the power in the device is off, thus imparting its nonvolatile characteristics. The suspended nanotube fabric and perpendicular trench electrode create a bistable structure that forms the basis of the memory element. When the fabric is suspended and relatively far from the electrode, a high junction resistance is read as a 0 or “OFF” state. When the fabric bends down and makes contact with the trench electrode, the corresponding junction resistance is orders of magnitude lower and is read as a 1 or “ON” state. The speed of these nanoscale switches is comparable to that of SRAM; however, the switches themselves can be patterned with the density of DRAM using standard CMOS and SOI lithography steps. Table 1 below outlines the main benefits of NRAM™ vs. existing memory technologies.

TABLE 1: NRAM™ BENEFITS

	NRAM™ Target	SRAM	DRAM	Flash
Cell Size	Comparable to DRAM	Large	Small	Small
Random Access	Comparable to SRAM	Fastest	Fast	Slow
Nonvolatile	Yes	No	No	Yes
Programming Voltage	<5 volts	NA	NA	> 10 volts
Active Power	Low	High	High	Medium
Standby Power	Zero	Low	High	Zero
Logic Process Integration	Low	Low	High	Very High
Complexity				
Scalability	Scalable	Limited	Limited	Limited

V. DESIGN FOR MANUFACTURABILITY

Nantero’s memory design and operating principle represent a technically elegant and innovative approach to storing memory bits. In addition, Nantero has overcome many of the fundamental manufacturing barriers through its R&D efforts and work with early adopters. The result is a scalable solution that leverages existing semiconductor manufacturing tools and processes.

1. Process Qualification

Nantero has perfected a purification process for a carbon nanotube formulation that meets production facility quality requirements. Nantero entered into a manufacturing relationship with Brewer Science to supply commercial scale quantities of purified carbon nanotube formulation to NRAM™ device manufacturers. LSI Logic and BAE Systems have introduced and qualified Nantero’s formulation into their respective production facilities in Gresham, Oregon and Manassas, Virginia. Nantero has also perfected a means to deposit and pattern its nanotube switches using industry standard photoresist spin tracks and lithography tools. This process can be done at room temperature, without harming preexisting circuitry. This eliminates the need for high temperature processing steps associated with chemical vapor deposition of the carbon nanotubes that can be detrimental to device reliability. In addition, a

Nanotechnology: Realizing the Promise of Universal Memory

manufacturer can leverage its existing tool investment and process methodology which reduces capital expenditures.

2. Process Compatibility

NRAM™ can be embedded into existing logic processes without additional process overhead by utilizing the same masks used for metallization and vias in a logic process. By embedding NRAM™ at the end of the production process, yields are also significantly improved.

3. Scalability

NRAM™ can scale with the minimum feature size in each technology node, and with a relative cell size significantly smaller than SRAM and comparable to DRAM, it will be able to deliver a greater density per silicon area than existing memory solutions.

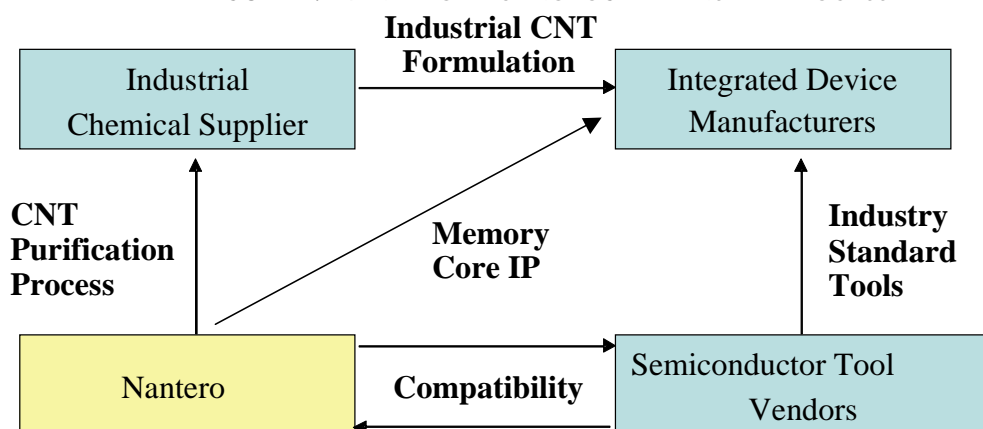
4. Reliability

Carbon nanotube switches are strong and resilient and do not wear out after a short number of cycles unlike other materials used for universal memory. In addition, carbon nanotubes retain their electrical characteristics through a wide range of temperatures.

5. Key Ecosystem Support for Technology Transfer

Commercializing new memory products based on advanced materials requires a technology transfer process from the R&D lab to the factory. This process becomes more difficult when moving technology know how between two separate entities. Nantero has addressed these challenges with NRAM™ by building an ecosystem of support partners to commercialize the product. These partners include Brewer Science, an established chemical supplier, ASML, an industry leading semiconductor tool manufacturer, and LSI Logic and BAE Systems, both large integrated device manufacturers. Each of these partners has contributed expertise toward developing a scalable and easily transferable manufacturing process for NRAM.™

FIGURE 2: NANTERO TECHNOLOGY TRANSFER PROCESS



VI. MEMORY MARKET FORECAST

Most electronics products in the market today utilize multiple types of memory. System designers across all sectors face the challenge of delivering more functionality at less cost in each new generation of product. Universal memory answers this challenge by integrating the key technical benefits of discrete memory products into one device resulting in higher system level performance, reduced unit costs, and increased reliability. These benefits are further realized in an embedded universal memory that integrates the memory function with logic on a shared die. The total market potential for universal memory can be defined as the aggregate of the all memory types, over \$150 billion in 2010.² Hard disk drive replacement with universal memory will add significantly to this total opportunity. Table 2 below shows the expected demand for total memory product in the semiconductor industry.

TABLE 2: EXPECTED DEMAND FOR TOTAL MEMORY PRODUCT IN SEMICONDUCTOR INDUSTRY

	2002	2003	2004	2005	2010	AAGR %
Total Memory Market	28.4	33.7	46.0	52.6	153.6	23.9%

Source: BCC, Inc.

Furthermore, the highest growth sectors of the memory market, portable consumer devices and smart appliances, especially benefit from the attributes of universal memory. For example, Gartner forecasts shipments in 2005 of 779 million handsets, growing to over one billion in 2009. Gartner also forecasts strong growth in smart phones through 2009, bringing total shipments to approximately 280 million handsets. The increased functionality of these phones drives the need for increased memory bandwidth and reduced active and standby power consumption. Embedding universal memory also increases security and programmability while reducing form factor, three features of increasing importance to the mobile device and smart appliance sectors.

VII. CONCLUSIONS

There are growing technical challenges to existing memory technology, while end markets will continue to drive strong demand for memory products that can concurrently deliver speed, density and nonvolatility. The universal memory that correctly meets these design and manufacturing constraints will have enormous market potential. The winning technology will satisfy this large market opportunity and leverage the existing manufacturing infrastructure and processes in the semiconductor industry to ensure smooth integration into existing and new end- products.

² *Id.*