NANTERO

White Paper
NRAM for Automotive Applications

NRAM Persistent Memory; A Revolutionary Advance for Automotive Applications

By Bill Gervasi

Abstract: Nantero NRAM® is a universal memory solution that provides enhanced performance, reliability, and security features for future generations of automotive designs. Key features include simplification of the designs, instant-on system reboots, operation and storage under wide temperature extremes, and enhanced security features including resistance to hacking. NRAM can replace the PROM, DRAM, and Flash currently used in system designs, improving system reliability. Performance is higher than DRAMs yet power is lower due to the reduced core traffic of a persistent memory array.

About the Author: Mr. Gervasi is Principal Systems Architect at Nantero, Inc. He has been working with memory devices and subsystems since 1Kb DRAM and EPROM were on the leading edge of technology. He has been a JEDEC leader since 1996, responsible for key introductions including DDR SDRAM, the integrated Registering Clock Driver and RDIMM architecture, the formation of the JEDEC committee on SSDs, and he chairs the emerging memories committee.

Introduction

Automobiles have long been evolving from mechanical devices to supercomputers on wheels, and reliance on electronic technologies is only increasing with each generation of vehicles. These electronics manage a wide variety of functions from engine control to various sensors to entertainment and communications. Artificial intelligence functions including driving assist are becoming commonplace in all vehicles. Combined, these electronic functions can generate hundreds of gigabytes of data per second.

Much of this data is used and discarded immediately. For example, information gathered from optical sensors is primarily about what objects are near the auto now rather than what was there a minute before. Streaming music may only choose to save the last few seconds of material for quick replay. However, there are critical data storage requirements that must be addressed. The control software for steering and braking, for example, must be active and valid at all times when the vehicle is operating.

For many years, three memory technologies were available to automotive designers: PROM, DRAM, and Flash. PROM is a low capacity non-volatile storage memory for the execution code for the system-on-a-chip (SoC) devices controlling the automotive functions, however, these memories are too slow for program execution so PROM contents are transferred to much faster but volatile DRAM to execute the control software. “Volatile” here means that when power is turned off, the content is destroyed. In particular, DRAM must be reloaded every time power is turned off then back on in a slow sequence generally called “reboot”. The third tier of memory, Flash, is also low performance but high capacity non-volatile memory used to save large amounts of data such as display images that can be reloaded when power is cycled.

Nantero NRAM® is a universal memory capable of replacing all tiers of memory storage. Like PROM or Flash, it retains its content even when power is turned off then back on. Like DRAM, it offers very high performance, allowing program execution directly from the NRAM. Because it functions as all tiers of memory, it eliminates the reboot time, offering true instant-on operation. NRAM can literally be a life-saving improvement in automotive design.

Automotive System Architecture

A simplified block diagram of a current-generation automotive control unit is shown in Figure 1. In this example, three SoCs are used for control: drive functions, communications, and entertainment. Each SoC has a dedicated PROM to contain boot code and dedicated DRAM for program execution. In this system, bulk Flash storage is a shared resource that all SoCs can access via a Hub device.

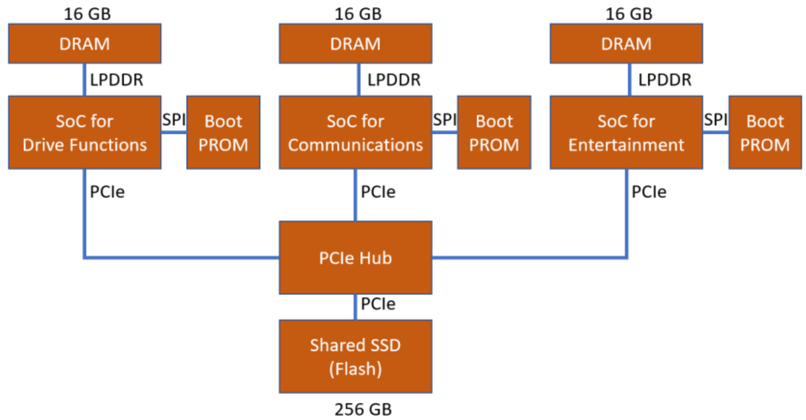

Figure 1: Automotive Control Using DRAM, PROM, and SSD

In the current-generation system model, system boot at power-on is a sequence that requires copying the boot code from the PROM to DRAM, executing the boot code to set up essential tables and execution variables prior to executing critical code functions such as engine control, steering, etc. Less critical functions, such as turning on the radio, are delayed and may require reloading extended code from the shared SSD before full runtime functionality is restored. Power may fail at any time, usually when the driver turns the vehicle off but also from unexpected sources such as a lightning strike disrupting normal execution. The system must provide a power fail warning to the SoC and provide sufficient energy resources for the SoC to save back to the SSD any data in process (radio station selected, etc). A vehicle boot process commonly takes up to 7 seconds to restore full functionality. Figure 2 shows this sequence graphically.

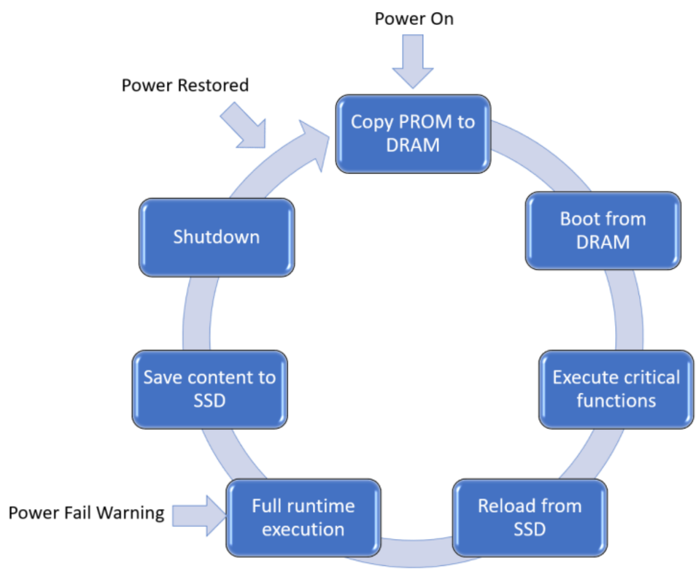

Figure 2: Traditional Boot-Run-Reboot Sequence

Nantero's solution simplifies this system architecture by replacing all PROM, DRAM, and SSD resources with NRAM as shown in Figure 3. The replacement of the volatile DRAM with non-volatile NRAM is an essential enabler for instant-on capability as it eliminates the boot or reboot processes completely. Full normal system operation is complete in microseconds. Once the NRAM is loaded with system code, it remains intact forever, including through power cycling whether intentional or due to external power fail effects.

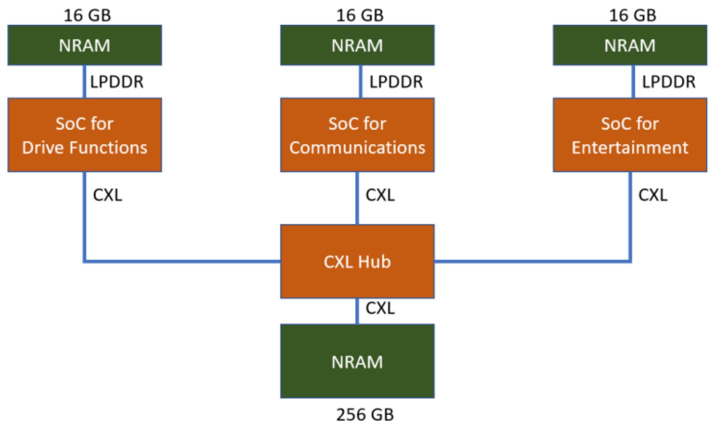

Figure 3: NRAM-based Automotive Control

In the proposed architecture, the PCIe bus typically used for SSDs is updated to use Compute Express Link (CXL), a lightweight protocol that uses PCIe for its physical layer but adds direct memory access functionality as well. This effectively expands the memory space for all SoCs in the system, and the use of shared data over CXL can eliminate redundant local storage in the memory attached to each SoC as well.

This results in a greatly simplified flow diagram for system execution. As shown in Figure 4, full runtime capability including critical and non-critical functions are available immediately upon normal power on or unintentional power failure and restoration. The only essential operation that needs to complete on power fail is that write operations in process to the NRAM must complete, a function that requires only nanoseconds to execute and therefore does not require an external energy source.

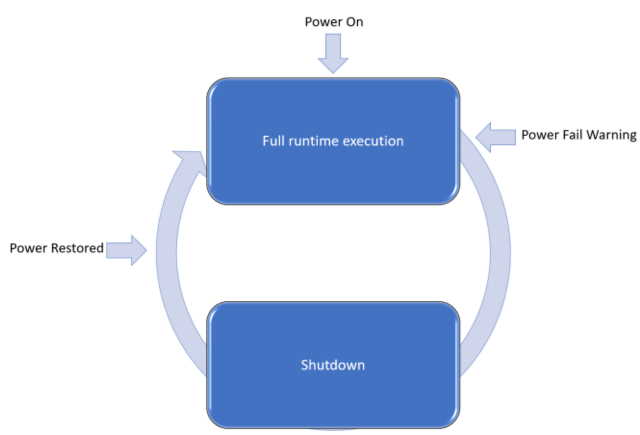

Figure 4: NRAM-enabled Instant-On Cycle

The process of checkpointing less critical data such as the user radio station selected in the previous example may be eliminated completely, as this information remains intact in the SoC-direct NRAM.

Performance and Power Benefits

NRAM's core memory array is inherently persistent. Once data is written, it is held for years with or without power. This persistence has interesting benefits for system performance as well. The most obvious benefit is the elimination of "Refresh", that DRAM-specific requirement that every 32 milliseconds, every cell of the DRAM must be read and rewritten; more often if temperatures get high. Refresh consumes 10-20% of available memory bandwidth. NRAM has no Refresh requirement, thereby offering 10-20% higher data throughput at the same clock frequency.

The elimination of Refresh makes the NRAM more SRAM-like in that it becomes fully deterministic. This allows controllers to reduce or eliminate internal buffers required to handle streaming data while the DRAM is busy with Refresh recovery.

A similar DRAM requirement that consumes performance is "Precharge". DRAM cores are emptied every time an Activate command reads the core content into an on-chip page buffer. After the data is used, even if only read and not written, this page buffer must be stored back into the DRAM core. NRAM has no need for Precharge since Activate does not erase the core. Also, Writes are limited to the data modified and need not write back an entire page buffer.

The combination of power savings from eliminating Refresh (11%) and Precharge (21%) makes NRAM a far lower power solution with 34% better performance per watt.

Reliability and Security Benefits

Simplification of the system design has intrinsic benefits in reliability as well. Fewer components result in fewer potential points of failure. Reducing the amount of data moving through the system, such as using the CXL NRAM as a shared direct-execute resource instead of copying content from Flash to DRAM, results in fewer communications errors.

NRAM solves at least one other critical requirement of automotive design: temperature sensitivity. Both DRAM and Flash memories are incapable of operating at high temperatures, and Flash loses content even when a vehicle is parked and turned off if it gets too hot. NRAM is based on carbon nanotubes which have an ideal thermal distribution coefficient and therefore are not affected by temperature extremes, hot or cold.

Automotive-grade DRAMs, for example, are typically rated from -40°C to +95°C, however temperatures under the hood of a vehicle can often exceed this range so designers are forced to employ cooling techniques to maintain the rated temperatures. SSDs with their internal Flash memories are even more restrictive, with an operation rating of -40°C to +85°C, further challenging system designers to keep the memory cool. Flash memory is also highly sensitive to power-off temperatures as well. As shown in Table 1, parking your car outside near a desert airport and going on vacation can result in data loss by the time you return home.

Table 1: Arrhenius Model for Flash Degradation Over Temperature

Storage °T	Acceleration Factor Relative to 55°C	Time Equivalent to 1 Year
85°C	26	360 hours (15 days)
70°C	5	1712 hours (71 days)
55°C	1	9390 hours (one year)
25°C	0.02	442,380 hours (50 years)

NRAM is rated from -55°C to +125°C, greatly simplifying system cooling and allowing more flexible placement in the vehicle. Data does not degrade under even the most extreme conditions.

Data security is increasingly essential in all devices and designing an intrusion-proof vehicle is an requisite design goal. NRAM solutions provide support for AES-512 level authentication and encryption. Every NRAM device provides a unique 40-bit serial number for SPDM validation and CXL NRAM controllers provide trusted supplier authentication and firmware resiliency mechanisms.

Many vehicles also allow the installation of apps in the vehicle. Examples include Alexa, Pandora, and iTunes. The capability to install apps increases the potential for harmful software to affect the integrity of vehicle operation, so vehicles must take aggressive measures to ensure invulnerability from software attacks. In particular, one significant weakness of DRAM-based systems is "Rowhammer" whereby a malicious program attempts to exploit a combination of cell droop over time and temperature with crosstalk caused by thousands of DRAM row activations imposing modification to nearby DRAM rows, shown graphically in Figure 5.

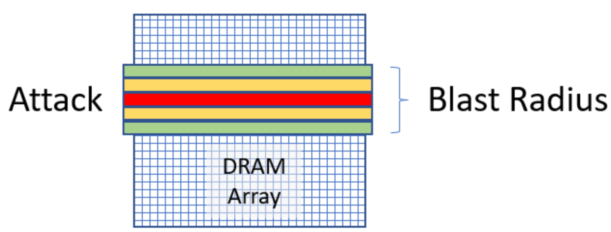

Figure 5: Rowhammer Attack on Adjacent DRAM Rows

NRAM also provides immunity from rowhammer attacks using a variety of internal architectural improvements over DRAM. These improvements prevent a malicious program from using this sensitivity to take control of a vehicle's operating environment.

Conclusion

In summary, using NRAM for automotive applications provides safer, more efficient vehicle operations. Instant-on capability enabled by the non-volatile and high-performance nature of NRAM means that vehicles can recover from catastrophic events such as nearby lightning strikes immediately, providing potentially life-saving restoration of vehicle control. NRAM provides a wide operating and storage temperature range, simplifying system design and ensuring long-term reliability.

NRAM systems enable high-security features for circuit validation and to prevent malicious intrusion into the system controls. NRAM as the universal memory solution reduces system complexity while providing vastly improved integrity of data and operating environments.

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